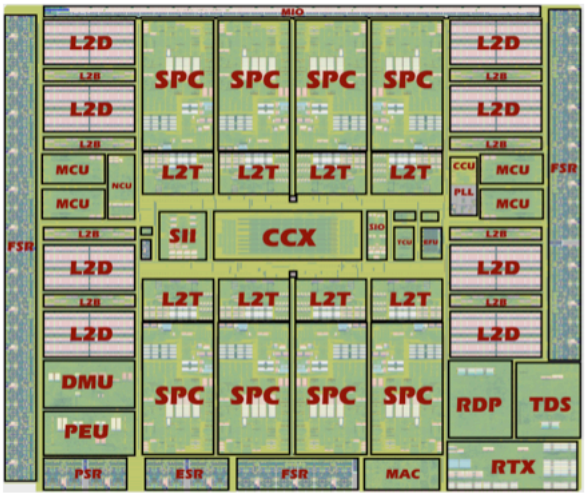
Niagara-2 Chip Overview

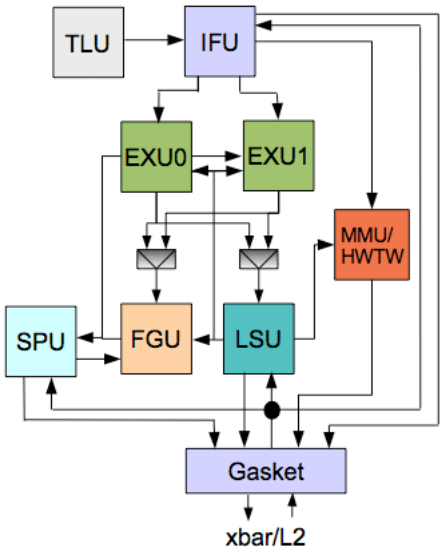


- 8 Sparc cores, 8 threads each
- Shared 4MB L2, 8-banks, 16-way associative
- Four dual-channel FBDIMM memory controllers
- Two 10/1 Gb Enet ports w/onboard packet classification and filtering
- One PCI-E x8 1.0 port
- 711 signal I/O, 1831 total

Glossary

- CCX – Crossbar
- CCU – Clock control
- DMU/PEU – PCI Express
- EFU – Efuse (redundancy)
- ESR – Ethernet SERDES
- FSR – FBDIMM SERDES
- L2B – L2 write-back buffers
- L2D – L2 Data
- L2T – L2 tags
- MCU – Memory controller
- MIO – Miscellaneous I/O
- PSR – PCI-Express SERDES
- RDP/TDS/RTX/MAC – Ethernet
- SII/SIO – I/O datapath in/out to memory
- SPC – Sparc core
- TCU – Test control unit

Sparc Core Block Diagram



- IFU – Instruction Fetch Unit
  - 16 KB I$, 32B lines, 8-way SA
  - 64-entry fully-associative ITLB
- EXU0/1 – Integer Execution Units
  - 4 threads share each unit
  - Executes one integer instruction/cycle
- LSU – Load/Store Unit
  - 8KB D$, 16B lines, 4-way SA
  - 128-entry fully-associative DTLB
- FGU – Floating/Graphics Unit
- SPU – Stream Processing Unit
  - Cryptographic acceleration
- TLU – Trap Logic Unit
  - Updates machine state, handles exceptions and interrupts
- MMU – Memory Management Unit
  - Hardware tablewalk (HWTW)
  - 8KB, 64KB, 4MB, 256MB pages