



	Logist	tics		
Lectures Instructor TA	T/Th 9:30-11:00, F Prof. William R. Ma Juhyun Lee	RAS 213 ark		
Grading	Final Exam Midterm Exam Homework Project	1 1 ~7 1	35% 25% 15% 25%	
Text	Hennessy & Patterson, <i>Computer</i> <i>Organization and Design</i> (Third Edition)			
UTCS	Lecture	1		3

	CS352 Online				
URL: www	.cs.utexas.edu/~billmark/ teach/cs352-07-spring	-			
email list:	cs352-mark@cs.utexas.edu subscribe by sending email to TA (mandatory - see web page for details)				
Computer Ar	Computer Architecture Seminar Series: www.cs.utexas.edu/users/cart/arch				
UTCS	Lecture 1 4				







Specification	compute the fibonacci sequence		
Program	for(i=2; i<100; i++) { a[i] = a[i-1]+a[i-2];}		
ISA (Instruction Set Architecture)	load r1, a[i]; CS 310, add r2, r2, r1; CS 352		
microArchitecture	CS 352		
Logic			
Transistors	⊣Ґ ➡ –ੈ ′		
Physics/Chemistry utcs I	I = C dV/dt Lecture 1 8		







































	Evaluation Tools		
 Benchmarks, traces, and a macrobenchmarks & application exection exection exection microbenchmarks microbenchmarks measure one aspection performance traces 	& mixes a suites MOVE BR ution time LOAD STORE ALU LD 5EA3	39% 20% 20% 10% 11%	
 replay recorded cache, branch, r Simulation at many le TSA cycle accurate 	accesses egister LD 1EA2 vels		1
 circuit trade fidelity for Area and delay estimation Analysis 	or simulation rate	→	٢
- e.g., queuing theory	-	•	



	Next Time	
 Evaluation of Performance Amdahl's Cost 	Systems e s Law, CPI	
 Computer system Transistors 	stem elements and wires	
 Reading assignment P&H Chapte 	gnment r 1	
UTCS	Lecture 1	30