CS 352 – Prof. Mark **Assignment #5** **Due March 29, 2007**

P&H 7.4

P&H 7.9

P&H 7.10

P&H 7.12

P&H 7.14

P&H 7.15 [10] <§7.2> Suppose a processor with a 16-word block size has an effective miss rate per instruction of 0.5%. Assume that the CPI without cache misses is 1.2. Using the memories described in Figure 7.11 on page 489 and Exercise 7.14, how much faster is this processor when using the wide memory than when using narrow or interleaved memories?

P&H 7.16

P&H 7.17 – 7.19 Average Memory Access Time

To capture the fact that the time to access data for both hits and misses affects performance, designers often use average memory access time (AMAT) as a way to examine alternative cache designs. Average memory access time is the average time to access memory considering both hits and misses and the frequency of different accesses; it is equal to the following:

AMAT = Time for a hit + Miss rate * Miss penalty

AMAT is useful as a figure of merit for different cache systems.

7.17 [5] <§7.2> Find the AMAT for a processor with a 2 ns clock, a miss penalty of 20 clock cycles, a miss rate of 0.05 misses per instruction, and a cache access time (including hit detection) of 1 clock cycle. Assume that the read and write miss penalties are the same and ignore other write stalls.

7.18 [5] <§7.2> Suppose we can improve the miss rate to 0.03 misses per reference by doubling the cache size. This causes the cache access time to increase to 1.2 clock cycles. Using the AMAT as a metric, determine if this is a good trade-off.

7.19 [10] <§7.2> If the cache access time determines the processor's clock cycle time, which is often the case, AMAT may not correctly indicate whether one cache organization is better than another. If the processor's clock cycle time must be changed to match that of a cache, is this a good trade-off? Assume the processors are identical except for the clock rate and the number of cache miss cycles; assume 1.5 references per instruction and a CPI without cache misses of 2. The miss penalty is 20 cycles for both processors.

P&H 7.25 [10] <§7.3> Using the series of references given in Exercise 7.9, show the hits

and misses and final cache contents for a two-way set-associative cache with one-word blocks and a *total size* of 16 words. Assume LRU replacement.

P&H 7.29

P&H 7.32