CS 352 – Prof. Mark **Assignment #3** **Due March 6, 2007**

Problems #1-12:

P&H 5.2

P&H 5.8

P&H 5.11

P&H 5.12

P&H 5.24:

> [5] <§§5.4, 5.5> A friend is proposing that the control signal MemtoReg be eliminated. The multiplexor that has MemtoReg as an input will instead use the control signal MemRead. Will your friend's modification work? Consider both datapaths.

P&H 5.26

> [15] <§5.4> Consider the following idea: Let's modify the instruction set architecture
> and remove the ability to specify an offset for memory access instructions. Specifically, all load-store instructions with nonzero offsets would become pseudoinstructions
> and would be implemented using two instructions. For example:
>
> ```
> addi  $at, $t1, 104     # add the offset to a temporary
> lw    $t0, $at          # new way of doing lw $t0, 104 ($t1)
> ```
>
> What changes would you make to the single-cycle datapath and control if this simplified architecture were to be used?

P&H 5.28

P&H 5.37

P&H 6.3

P&H 6.4

P&H 6.5

> [5] <§6.1> How could we modify the following code to make use of a delayed branch slot?
>
> ```
> Loop: lw    $2, 100($3)
>       addi  $3, $3, 4
>       beq   $3, $4, Loop
> ```

P&H 6.6