Computer Organization and Design, The Hardware/Software Interface, Third Edition

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Errata list as of 1/20/05

Chapter		Page #	Description
Preface		xiii	Chart: Several section numbers wrong. Ex: "3.1 to 3.11" --> "3.1 to 3.9"
		xiv	Line 20: progams --> programs
	1	18	Margin, "pixel": "Screen are…" --"Screens are…"
	1	20	3rd paragraph: "The processor is the large square below the memory boards in the lower-right corner of Figure 1.8…" --> "The processor is under the fan and covered by a heat sink on the left side of Figure 1.8"
		21	Figure 1.9: Label missing from top of figure. Should read "Misc. interface logic"
	1	23/24	Last sentence of pg 22 refers to "Big Picture". The Big Picture section (pg. 24) should be at top of page 23.
	1	23	Sidebar definition, volitile memory: "Storage, such as DRAM, that only retains…" --> "Storage , such as DRAM, that retains…"
	2	69	Figure 2.9 caption: Additional line: "MIPS implements NOT using a NOR with one operand being zero.
	2	71	Figure 2.10: "srl $$s1,$s2,10" --> "srl $s1,$s2,10"
	2	73	Figure 2.11: I ^ j --> I=/=j?
	2	75	Line 4: "add $s3…" --> "addi $s3…"
	2	75	Line 13: "...program into basic blocks" --> "…program into basic blocks."
	2	77	Figure 2.12, logical: "srl $$s1,$s2,10" --> "srl $s1,$s2,10"
	2	77	Figure 2.12, conditional branch: slt --> slti
	2	84	7th line from bottom: addi$a0,$a0 --> addi $a0,$a0
	2	84	6th line from bottom: jalfact --> jal fact
	2	88	Line 2: "…to a 'dangling pointers'…" --> "..to 'dangling pointers'…"
	2	89	Figure 2.19: "srl $$s1,$s2,10" --> "srl $s1,$s2,10"
	2	89	Figure 2.19, conditional branch: slt --> slti
	2	90	Sidebar quote: “(“ --> “(” use closed quote instead of open quote
	2	99	Answer Table
	2	101	Figure 2.24: In subparts 3 and 4, the line from "rs" to "+" should go from "address" to "+".

Chapter	Page #	Description
2	102	Line 6: The label for bit 2 is over bit 3 instead of bit 2.
2	108	Line 5: "MIPS assemblers use hexadecimal," --> "MIPS assemblers use hexadecimal."
2	152	Table: clear $t50 --> clear $t0
2	153	Last line: "on page 141" --> "on page 146"
3	166	Line 10 & 11: There should be a bar over the second X in the first two equations, and over the first X in the last one.
3	168	7th line from bottom: "…also illustrated on the back endpapers of this book' --> "..also illustrated on the green card at the front of the book"
3	168	2nd line from botttom: "String" in normal font because There is no string type in C, and wide strings can use 2 bytes per character.
3	182	Figure 3.9: You need 31 adders, not 32, and Product0 is the rightmost bit of Mplier0.Mcand. What is labeled Product0 is actually Product1. And the leftmost input to the 31st (bottom) adder is Multiplier31.Mcand, not Multiplier3.Mcand.
3	197	Line 7: "... as noted in Section ." --> ""... as noted in section 3.6."
3	197	Elaboration: Additional line: "Recent IBM mainframes support IEEE755 as well as hex format.
3	209	2nd Paragraph: "…single internal format" --> "single internal format."
4	269	3rd line from bottom: In equation MIPS2, remove (30) in denominator.
4	273	Exercise 4.10: Table uses the old terms M1 and M2, but should be I1 and I2.
4	281	Column 2, line 7: deacceleration --> deceleration
5	286	5th paragraph, line 2: "insrtuction" --> "instruction"
5	302	Last line: "shows how the 3-bit..." --> "shows how the 4-bit..."
5	314	Figure 5.24: the vertical line connecting MemRead from Control to Data memory is missing
5	322	Figure 5.27: Output of Memory data register connection is missing. It should have a connection to position 1 of the Mux for Write data of Registers
	322	Figure 5.27: Mux with input ALUSrCA does not have any input tied to the one labeled as "0". This one should come from the PC
5	339	Figure 5.38, State 4: "RegDst = 1" --> "RegDst = 0"
	339	Figure 5.38, State 4: "MemtoReg = 0" --> "MemtoReg = 1"
5	355	Exercise 5.14, Line 6: "care" --> "case"
5	356	Exercise 5.29 should refer to Fig 5.28, not Fig 5.27.
5	357	Exercise 5.32: "15]" --> "[15]"
6	397	Figure 6.19, Time (in Clock cycles): CC6 CC1 CC2 CC3 --> CC6 CC7 CC8 CC9

Chapter	Page #	Description
	397	Figure 6.20, Time (in Clock cycles): CC6 CC1 CC2 CC3 --> CC6 CC7 CC8 CC9
6	409	Figure 6.30b: There should be a third input to the top Mux. It should come from the ID/EX
	411	Figure 6.32: There should be a third input to the top Mux. It should come from the ID/EX
6	412	Figure 6.33: There should be a third input to the top Mux. It should come from the ID/EX
6	415	Figure 6.35: "add $4, $2, $5" --> "and $4, $2, $5"
6	427	Figure 6.41: "EX/MEM" --> "MEM/WB"
6	465	Figure: October capitalized
7	550	Figure: "Cache block number" should be centered under three bits 0 0 1 numbered 7 to 5
	550	Figure: "Block offset number" should be centered under five bitts 0 1 1 0 0 numbered 4 to 0
8	577	Figure 8.7: D0xx and Pxx should be D0' and P0'. (In the figure, the "xx" looks like two squares)
CD		
CD Sections	2.12-6	Figure: 2.12.4: Code motion is applied to move the "LW R6, k" outsode of the loop. However, R6 is later overwritten by variable I in "LW R6, I" such that the while test is performed on variable I instead of variable k in "BEQ R5, R6, startwhileloop".
appendix B	B-7	Equation: "...assign E - A ^ B ^ C, D" --> "…assign E = (A ^ B ^ C) * (A + B + C) * (A * B * C) which is yet another way to describe this function. D and F have even simpler…"
	B-8	Sidebar: a decoder with n-bit input has 2^n outputs, not 2n outputs
	B-21	3rd line from bottom: "specifies a variable register file that ..." --> "specifies a variable registerfile that ..."
	B-22	2nd line from bottom: "{{4{1'b1}},{4{1'b1}}}" --> "{{4{1'b1}},{4{1'b0}}}"
	B-22	Second bullet: ""z, representing unkown, ..." --> "x, representing unknown, ..."
	B-37	Figure B.5.16: Outputs should be ALUCt1, not ALUOp, which is input.
	B-42	Figure B.6.2: Top part of figure has an extra wrench handle in the middle.
	B-58	First paragraph: "2M = 2^22" --> "4M = 2^22"
	B-61	Figure B.9.3 caption: The caption has a Yen sign where there should be an x, as in "4 x 2 SRAM
	B-62	Figure B.9.4 caption: Yen sign instead of a x in the caption (should be "4M x 8 SRAM")
	B-62	(Page 62) --> Page B-62
Glossary	G-11	First line, second column: "alway" -->"always"
Green Card	1	In the shift left and right instructions the rs field is suppose to be set to zero (see page 69) yet the green card in the front of the book is different. It shows rs as the source to be shifted. I am pretty sure that rs = zero since SPIM assembles the code that way.

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	2	Under MIPS reference data for load word (lw) instruction: 0/23hex --> 23hex